ISO 9001 Registered

IMP5111/5112

9-Line SCSI Terminator

–35MHz Channel Bandwidth

DESCRIPTION

The IMP5111/5112 SCSI terminators are part of IMP's SCSI terminator family of high-performance, adaptive, non-linear mode SCSI products, which are designed to deliver true UltraSCSI performance in SCSI applications. The low voltage BiCMOS architecture employed in their design offers performance superior to older linear passive and active techniques. IMP's SCSI terminator architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible — typically 35MHz, which is 100 times faster than the older linear regulator/ terminator approach used by other manufacturers. Products using this older linear regulator approach have bandwidths which are dominated by the output capacitor and which are limited to 500KHz (see further discussion in the Functional Description section). This new architecture also eliminates the output compensation capacitor required in earlier terminator designs. Each is approved for use with SCSI-1, -2, -3, UltraSCSI and beyond — providing the highest performance alternative available today.

Another key improvement offered by the IMP5111/5112 lies in their ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as the use of improper cable lengths and impedances. Frequently, this situation is not controlled by the peripheral or host designer and, when problems occur, they are the first to be made aware of the problem. The IMP5111/5112 architecture is much more tolerant of marginal system integrations.

Recognizing the needs of portable and configurable peripherals, the IMP5111/5112 have a TTL compatible sleep/disable mode. Quiescent current is typically less than 275µA in this mode, while the output capacitance is also less than 3pF. The obvious advantage of extended battery life for portable systems is inherent in the product's sleep-mode feature. Additionally, the disable function permits factory-floor or production-line configurability, reducing inventory and product-line diversity costs. Field configurability can also be accomplished without physically removing components which, often times results in field returns due to mishandling.

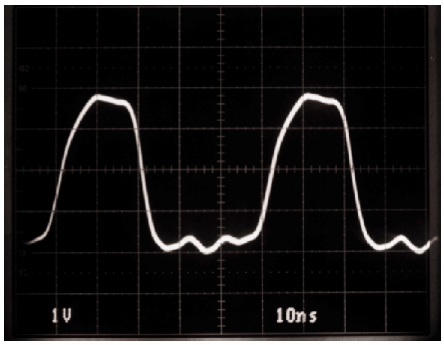
Reduced component count is also inherent in the IMP5111/5112's architecture. Traditional termination techniques require large stabilization and transient protection capacitors of up to 20µF in value and size. The IMP5111/5112 architecture does not require these components, allowing all the cost savings associated with inventory, board space, assembly, reliability, and component costs.

KEY FEATURES

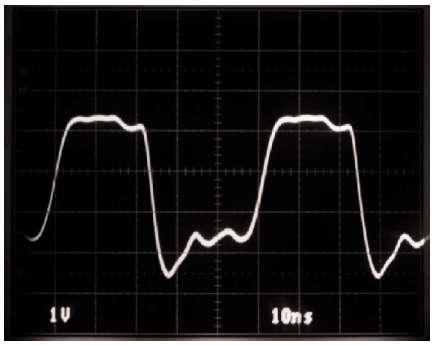
- ULTRA-FAST RESPONSE FOR FAST-20 SCSI APPLICATIONS
- 35MHz CHANNEL BANDWIDTH
- 3.3V OPERATION
- LESS THAN 3pF OUTPUT CAPACITANCE
- SLEEP-MODE CURRENT LESS THAN 275µA
- THERMALLY SELF LIMITING
- NO EXTERNAL COMPENSATION CAPACITORS
- IMPLEMENTS 8-BIT OR 16-BIT (WIDE) APPLICATIONS
- COMPATIBLE WITH ACTIVE NEGATION DRIVERS (60mA / CHANNEL)
- COMPATIBLE WITH PASSIVE AND ACTIVE TERMINATIONS
- APPROVED FOR USE WITH SCSI 1, 2, 3 AND ULTRA SCSI
- HOT SWAP COMPATIBLE
- PIN-FOR-PIN COMPATIBLE WITH LX5211 AND UC5606 (IMP5111)
- PIN-FOR-PIN COMPATIBLE WITH LX5212 AND UC5603/5613/5614 (IMP5112)

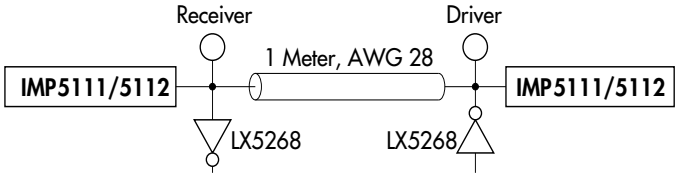
PRODUCT HIGHLIGHT

RECEIVING WAVEFORM - 20MHz



DRIVING WAVEFORM - 20MHz





PACKAGE ORDER INFORMATION

T_A (°C)	DP Plastic SOIC 16-pin, Power	PWP Plastic TSSOP 24-pin, Power
0 to 125	IMP5111CDP	IMP5111CPWP
	IMP5112CDP	IMP5112CPWP

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. IMP5111CDPT)

ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current 0.4A
Operating Junction Temperature
Plastic (DP, PWP Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

DPj PACKAGE:

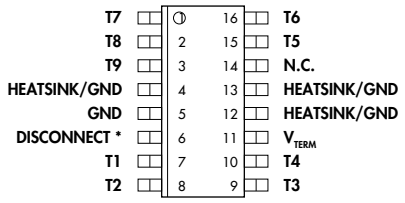
THERMAL RESISTANCE-JUNCTION TO LEADS, Q_{JL} ..... 20°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Q_{JA} ..... 50°C/W

PWP PACKAGE:

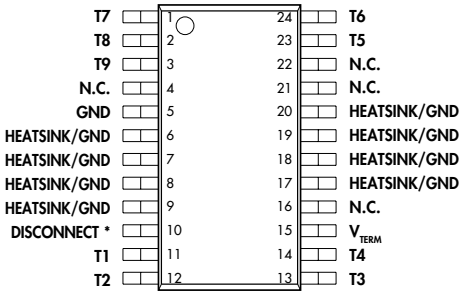
THERMAL RESISTANCE-JUNCTION TO LEADS, Q_{JL} ..... 27°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Q_{JA} ..... 100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow.

PACKAGE PIN OUTS



DP PACKAGE
(Top View)



PWP PACKAGE
(Top View)

*$\overline{\text{DISCONNECT}}$ for the IMP5112,
and **DISCONNECT** for the IMP5111.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter		Symbol	Recommended Operating Conditions			Units
			Min.	Typ.	Max.	
Termination Voltage		V_{TERM}	3.3		5.5	V
High Level Enable Input Voltage	IMP5111	V_{IH}	2		V_{TERM}	V
	IMP5112		0		0.8	V
Low Level Disable Input Voltage	IMP5111	V_{IL}	0		0.8	V
	IMP5112		2		V_{TERM}	V
Operating Virtual Junction Temperature Range						
IMP5111C/5112C			0		125	°C

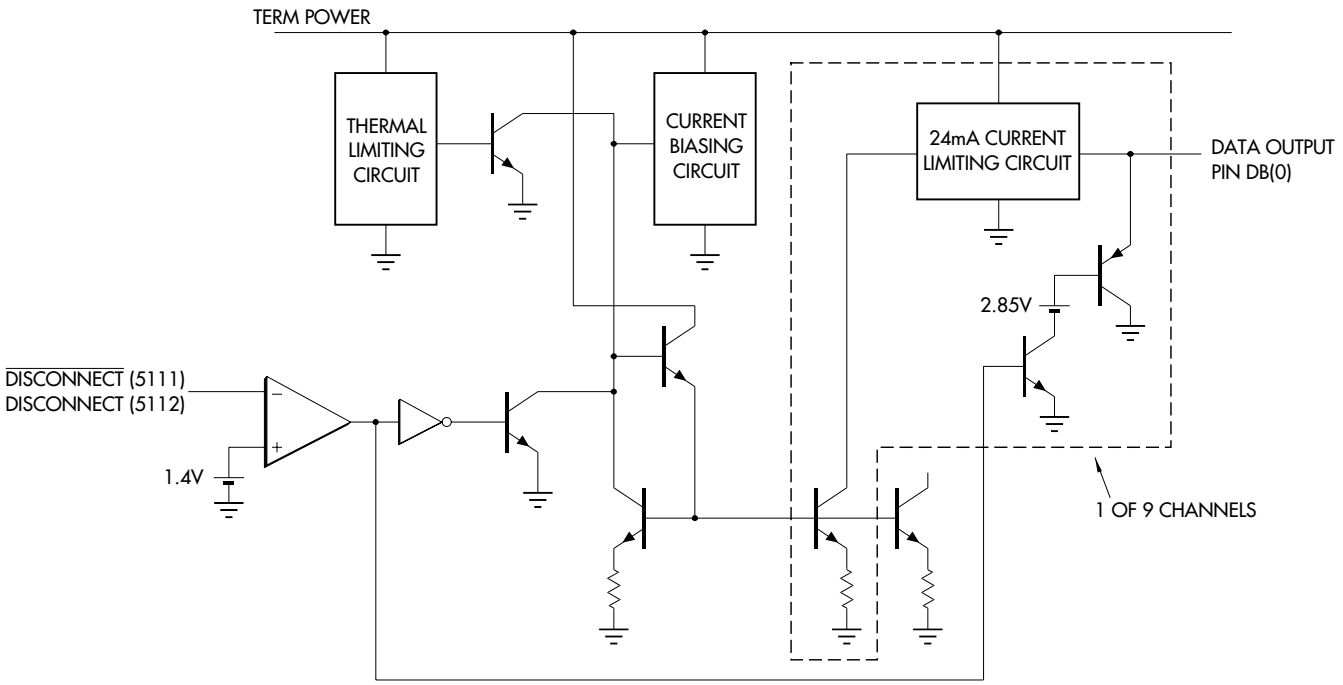
Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

Term Power = 4.75V unless otherwise specified. Unless otherwise specified, these specifications apply at the recommended operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter		Symbol	Test Conditions	LX5111/5112			Units
				Min.	Typ.	Max.	
Output High Voltage		V_{OUT}		2.65	2.85		V
TermPwr Supply Current		I_{CC}	All data lines = open		6	9	mA
			All data lines = 0.5V		215	225	mA
	IMP5111		$\overline{\text{DISCONNECT}}$ Pin < 0.8V		275		µA
	IMP5112		DISCONNECT Pin > 2.0V		275		µA
Output Current		I_{OUT}	V_{OUT} = 0.5V	-21	-23	-24	mA
DISCONNECT Input Current	IMP5111	I_{IN}	$\overline{\text{DISCONNECT}}$ Pin = 4.75V		10		nA
			$\overline{\text{DISCONNECT}}$ Pin = 0V		-90		µA
DISCONNECT Input Current	IMP5112	I_{IN}	DISCONNECT Pin = 0V		-90		µA
			DISCONNECT Pin = 4.75V		10		µA
Output Leakage Current	IMP5111	I_{OL}	$\overline{\text{DISCONNECT}}$ Pin = < 0.8V, V_O = 0.5V		10		nA
	IMP5112		DISCONNECT Pin = > 2.0V, V_O = 0.5V		10		nA
Capacitance in DISCONNECT Mode		C_{OUT}	V_{OUT} = 0V, frequency = 1MHz		3		pF
Channel Bandwidth		BW			35		MHz
Termination Sink Current, per Channel		I_{SINK}	V_{OUT} = 4V		60		mA

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators, which consist of Linear Regulators in series with resistors (typically 110Ω), are a compromise. As the line voltage increases, the amount of current decreases linearly by the equation V = I * R. The IMP5111/5112, with their unique new architecture applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Acting as a near ideal line terminators, the IMP5111/5112 closely reproduce the optimum case when the devices are enabled. To enable the device the DISCONNECT pin (DISCONNECT pin for the IMP5112) must be pulled logic **High** (logic **Low** for the IMP5112). During this mode of operation, quiescent current is 6mA and the devices will respond to line demands by delivering 24mA on assertion, and by imposing 2.85V on deassertion. In order to disable the device, the DISCONNECT pin (DISCONNECT pin for the IMP5112) must be driven logic **Low** (logic **High** for the IMP5112). This mode of operation places the devices in a sleep state where a meager 275µA of quiescent current is consumed. Additionally, all outputs are in a Hi-Z (impedance) state. Sleep mode can be used for power conservation or to completely eliminate the terminator from the SCSI chain. In the second case, termination node capacitance is important to consider. The terminators will appear as a parasitic distributed capacitance on the line, which can detract from bus performance. For this reason, the IMP5111/5112 have been optimized to have only 3pF of capacitance per output in the sleep state.

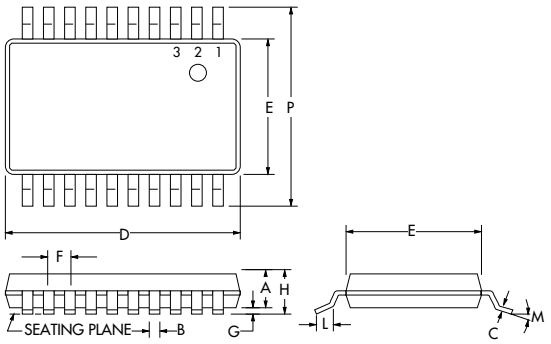
An additional feature of the IMP5111/5112 IC's are their compatibility with active negation drivers. These devices handle up to 60mA of sink current for drivers which exceed the 2.85V output high.

POWER UP / POWER DOWN FUNCTION TABLE

IMP5111 DISCONNECT	IMP5112 DISCONNECT	Outputs	Quiescent Current
H	L	Enabled	6mA
L	H	HI Z	275µA
Open	Open	HI Z	275µA

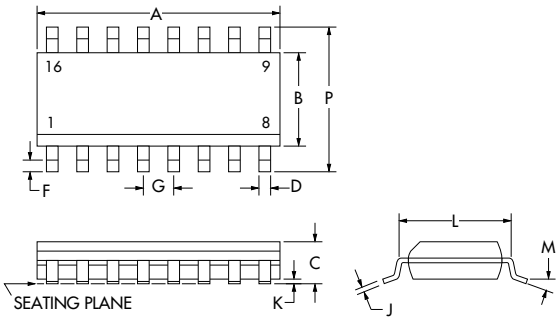
PACKAGE DIMENSIONS

PWP 24-Pin TSSOP
POWER



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.73	1.99	0.068	0.078
B	0.25	0.38	0.009	0.015
C	0.13	0.22	0.005	0.008
D	7.70	7.90	0.303	0.311
E	5.20	5.38	0.205	0.212
F	0.65 BSC		0.025 BSC	
G	0.05	0.21	0.002	0.008
H	1.63	1.83	0.064	0.072
L	0.65	0.95	0.025	0.037
M	0°	8°	0°	8°
P	7.65	7.90	0.301	0.311

DP 16-Pin Plastic SOIC
POWER



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.51	0.77	0.020	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.10	0.25	0.004	0.010
L	4.82	5.21	0.189	0.205
M	0°	8°	0°	8°
P	5.79	6.20	0.228	0.244

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